REMARKS

Applicants would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office Action, and this paper in response thereto. Reconsideration and withdrawal of all grounds of rejection are respectfully requested in view of the following remarks.

Claims 1–44 remain in this application. Claims 31–42 stand allowed. No claims have been amended.

The Examiner objects to the drawings for not showing every feature of the invention specified in the claims. In particular, the Examiner states that he is not sure how the configuration bit shown in the drawings could control rows and columns, where each configuration bit is exclusively associated with one or more of the plurality of display outputs. The Examiner also urges applicants to explain more about how the independent claims are enabled. For the following reasons, the Examiner's objection is traversed.

37 CFR §1.83(a) states that the "conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)". Datasheets are enclosed with this response showing examples of configurable drivers that, although different than the invention as claimed, show the level of skill in the art. One skilled in the art would know how to implement the described embodiments of the invention with the drawings and accompanying descriptions found in the application in view of the configurable drivers disclosed in the datasheets. Accordingly, it is respectfully submitted that applicants have complied with the rule, and no new drawings are necessary.

Applicants' specification and drawings sufficiently describe how to implement Applicants' claimed invention. For example, Figures 2-6 all show various embodiments of the invention where configuration bits are shown as R/C or R/C_n. The accompanying text makes clear that the configuration bits are associated with one or more outputs, such that when the bit is set to one value, the one or more outputs will drive a row on a display, but when the bit is set with another value, the one or more outputs will drive a column of the display (see, e.g., paragraphs 0039-0057). Figures 4-6 support embodiments where the outputs are grouped into blocks, with one configuration bit controlling the status of the entire block, such that when the bit of the block is set to one value, all of the outputs of the block

are set to drive rows, and when the bit is set to another value, all of the outputs of the block are set to drive columns (see, e.g., paragraphs 0041-0042).

There is no requirement that drawings be provided for every conceivable embodiment or every detail of the embodiments described in the application. It is well established that a patent application need not be a production document. Nor is there any requirement for Applicants to build a driver or include examples describing its operation. Applicants have complied with the 35 U.S.C. §112 in that the application describes the manner and process of making and using the invention in terms sufficient to enable one of ordinary skill in the art to make and use the invention. Accordingly, it is submitted that the drawings are satisfactory and that no changes are required.

Applicants are unaware of any authority in the patent statute or rules for the statement in the Office Action that the drawings should be amended and if not, the application will be abandoned. The Examiner is requested to contact the undersigned to clarify this point. In any event, it is respectfully submitted that no drawing changes are necessary for the reasons discussed above. Withdrawal of the objection to the drawings is respectfully requested.

Claims 1–3, 6–9, 12–15, 27–30, 43, and 44 were rejected under 35 U.S.C. §102(e) as being anticipated by Awamoto *et al.* (U.S. 6,452,590). Claims 4, 5, 10, 11, 16, 17 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Awamoto in view of Yang (U.S. 6,154,190). For the following reasons, the rejections are respectfully traversed.

Claim 1 recites, *inter alia*, a "plurality of display outputs each for outputting a drive voltage to a row or a column of a display" and a plurality of "configuration bits each having a row/column setting" wherein "each configuration bit is exclusively associated with one or more of said plurality of display outputs such that said row/column setting of said configuration bit is used to configure all of said associated one or more display outputs for driving either rows or columns of the display." The remaining rejected independent claims, and new claim 43, while having different scope, also recite limitations to configuration bits and configurable outputs. The cited reference does not disclose these claim limitations.

The Examiner cites Awamoto as disclosing outputs that can be configured to drive either rows or columns, in particular, address driver 29. However, it is clear that the reference discloses only that address driver circuit 29 drives columns of the display 10 (see Fig. 1, and col. 7, lines 6-9, 12-14). The reference discloses only an X driver circuit 27 and a Y driver circuit 28 for driving rows, and the address driver circuit 29 for driving columns (see

also Fig. 1). Awamoto fails to disclose that any driver output can be configured for driving "either rows or columns of the display" based on a configuration bit setting as claimed. Accordingly, claim 1 is patentably distinguished from Awamoto.

The remaining claims are patentable over Awamoto for either incorporating limitations to configuration bits and/or configurable outputs, or by their dependency upon claim 1.

Finally, the Office Action has failed to establish a *prima facie* case of obviousness with regard to claims 4, 5, 10, 11, 16, 17 and 26. Even assuming, *arguendo*, that the references would have been combined, Yang does not compensate for the deficiencies of Awamoto. Accordingly, it is respectfully submitted that this rejection for obviousness should be withdrawn.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. The Examiner is invited to telephone the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 35835US1.

Respectfully submitted,
PEARNE & GORDON, LLP

By: _____
Robert F. Bodi – Reg. No. 48,540

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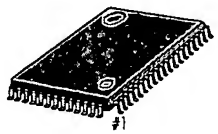
(216) 579-1700

Date: March 28, 2006

INTRODUCTION

The KS0065B is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 20 x 2bit bi-directional shift register, 20 x 2bit data latch and 20 x 2bit driver. (refer to Fig 1) This LSI can be used as common or segment driver.

64 QFP-1420F



FUNCTION

- Dot matrix LCD driver with 40 channel output.
- Selects function to use common/segment drivers simultaneously.
- Input / Output signal
  - output : 20 x 2 channel waveform for LCD driving
  - input : - Serial display data and control signal from the controller LSI.
    - Bias voltage (V_1~V_6)

FEATURES

- Display driving bias : static~1/5
- Power supply voltage : 2.7 ~ 5.5V
- Supply voltage for display : 3.0 ~ 13.0V (V_{LCD}=V_{DD}-V_{EE})
- Interface

Driver (cascade connection)	Controller
Other KS0065B, KS0063B	KS0066U KS0070B KS0073

- CMOS Process
- 64QFP and bare chip available

BLOCK DIAGRAM

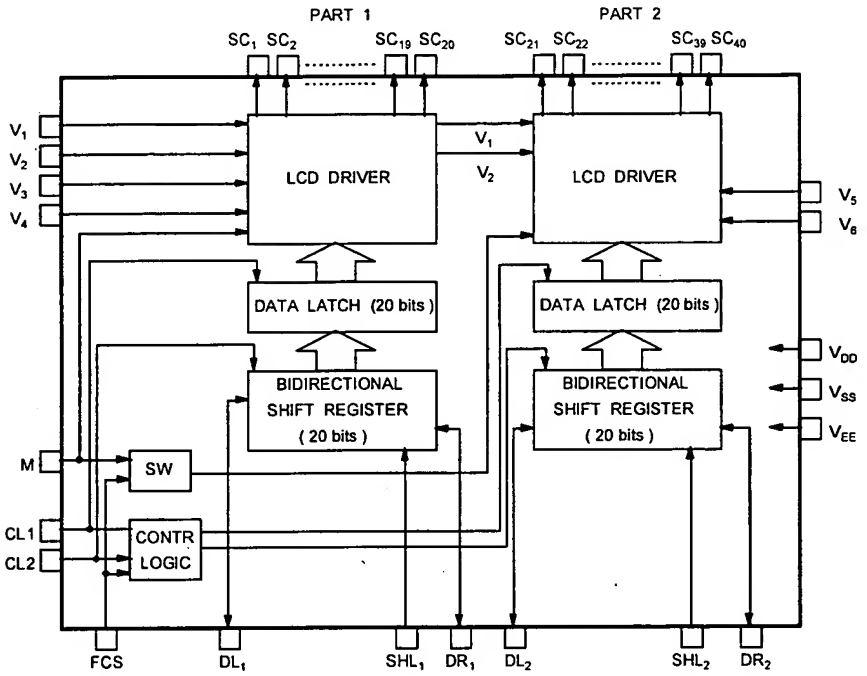


Fig 1. KS0065B functional block diagram

PIN CONFIGURATION

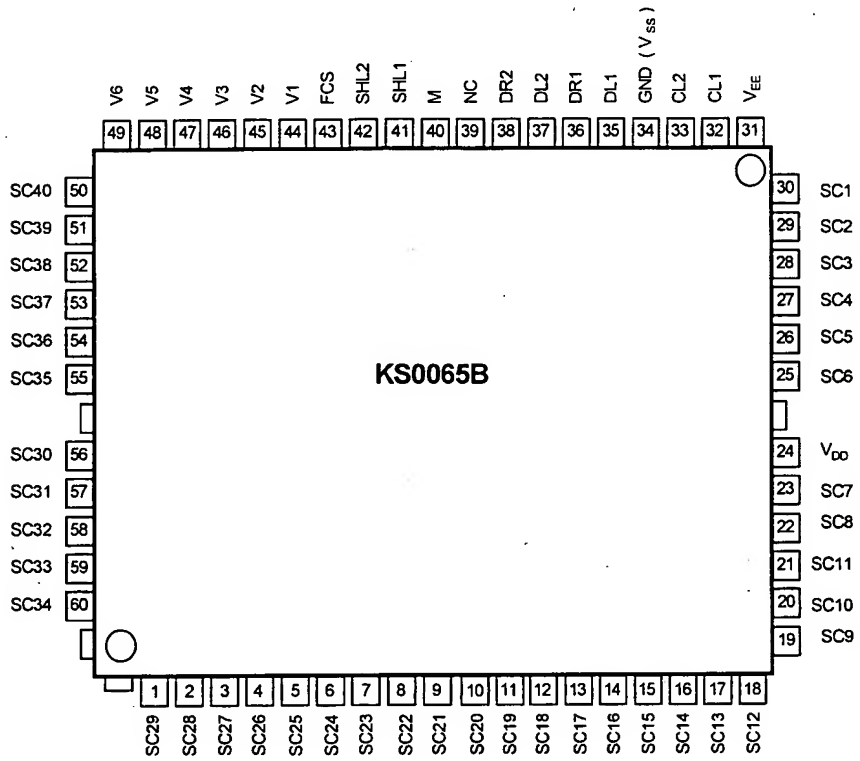
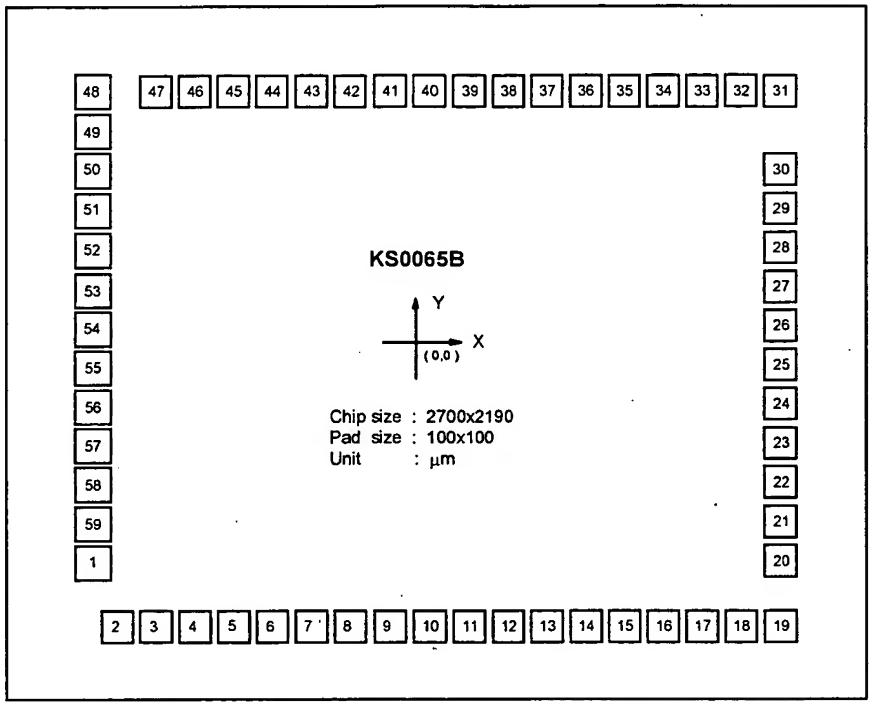


Fig 2. 60 QFP Top View

PAD DIAGRAM



Note : (0,0) is center in the chip

PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y
1	VEE	-1120.2	-642.5	31	SC28	1117.5	865.2
2	CL1	-1062.5	-865.2	32	SC27	992.5	865.2
3	CL2	-937.5	-865.2	33	SC26	867.5	865.2
4	VSS	-812.5	-865.2	34	SC25	742.5	865.2
5	DL1	-687.5	-865.2	35	SC24	617.5	865.2
6	DR1	-562.5	-865.2	36	SC23	492.5	865.2
7	DL2	-437.5	-865.2	37	SC22	367.5	865.2
8	DR2	-312.5	-865.2	38	SC21	242.5	865.2
9	M	-187.5	-865.2	39	SC20	117.5	865.2
10	SHL1	-62.5	-865.2	40	SC19	-7.5	865.2
11	SHL2	62.5	-865.2	41	SC18	-132.5	865.2
12	FCS	187.5	-865.2	42	SC17	-257.5	865.2
13	V1	332.5	-865.2	43	SC16	-382.5	865.2
14	V2	457.5	-865.2	44	SC15	-507.5	865.2
15	V3	582.5	-865.2	45	SC14	-632.5	865.2
16	V4	707.5	-865.2	46	SC13	-757.5	865.2
17	V5	832.5	-865.2	47	SC12	-882.5	865.2
18	V6	957.5	-865.2	48	SC9	-1120.2	857.2
19	SC40	1082.5	-865.2	49	SC10	-1120.2	732.5
20	SC39	1120.2	-627.5	50	SC11	-1120.2	607.5
21	SC38	1120.2	-502.5	51	SC8	-1120.2	482.5
22	SC37	1120.2	-377.5	52	SC7	-1120.2	357.5
23	SC36	1120.2	-252.5	53	VDD	-1120.2	232.5
24	SC35	1120.2	-127.5	54	SC6	-1120.2	107.5
25	SC30	1120.2	-2.5	55	SC5	-1120.2	-17.5
26	SC31	1120.2	122.5	56	SC4	-1120.2	-142.5
27	SC32	1120.2	247.5	57	SC3	-1120.2	-267.5
28	SC33	1120.2	372.5	58	SC2	-1120.2	-392.5
29	SC34	1120.2	497.5	59	SC1	-1120.2	-517.5
30	SC29	1120.2	622.5				

PIN DESCRIPTION

<table>
<tr><th>PIN(NO.)</th><th>INPUT/ OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(24)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (2.7 ~ 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(34)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V_1, V_2 (44,45)</td><td>Input</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC_1~SC_{20}</td><td>Output</td><td rowspan="3">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V_3, V_4 (46, 47)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL1 (41)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1 (35, 36)</td><td>Input Output</td><td>Data input/output of Part 1 shift register</td><td>Controller or KS0065B</td></tr>
<tr><td>SC_{21}~SC_{40}</td><td>Output</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V_5, V_6 (48, 49)</td><td>Input</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL2 (42)</td><td>Input</td><td>Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2 (37, 38)</td><td>Input Output</td><td>Data input/output of Part 2 shift register</td><td>Controller or KS0065B</td></tr>
<tr><td>M (40)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polarity</th></tr><tr><td rowspan="2">1</td><td>VSS</td><td rowspan="2">latch clock</td><td rowspan="2">shift clock</td><td>M</td></tr><tr><td>VDD</td><td rowspan="2">$\overline{M}$</td></tr><tr><td>2</td><td>VSS</td><td rowspan="2">shift clock</td><td rowspan="2">latch clock</td></tr><tr><td>VDD</td></tr></table>Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td><td rowspan="3">Controller</td></tr>
<tr><td>CL1,CL2 (32,33)</td><td>Input</td><td colspan="2">Data shift /latch clock</td></tr>
<tr><td>FCS(43)</td><td>Input</td><td colspan="2">Mode selection</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>N.C</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (T_a=25 °C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3 ~ +7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD}-15.0 ~ V_{DD}+0.3	V
Input Voltage 1	V_{IN1}	-0.3 ~ V_{DD}+0.3	V
Input Voltage 2 (V_1-V_6)	V_{IN2}	V_{DD}+0.3 ~ V_{EE}-0.3	V
Operating Temperature	T_{OPR}	-30 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

* Voltage greater than above may damage the circuit
* V_{EE} : connect a protection resistor (220Ω±5%)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=2.7 ~ 5.5V, V_{DD}-V_{EE}=3 ~ 13V, V_{SS}=0V, T_a= -30 ~ +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2}=400KHz	-	1	mA	-
Supply Current *	I_{EE}	f_{CL1}=1KHz	-	10	µA	
Input High Voltage	V_{IH}	-	0.7 V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2
Input Low Voltage	V_{IL}		0	0.3 V_{DD}		DR1, DR2, SHL1, SHL2
Input Leakage Current	I_{LKG}	V_{IN}=0-V_{DD}	-5	5	µA	M, FCS
Output High Voltage	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL}=+0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON}=0.1mA for one of SC1-SC40	-	1.1		$V(V_1-V_6)$-SC(SC1-SC40)
	V_{D2}	I_{ON}=0.05mA for each SC1-SC40	-	1.5		
Leakage Current	I_V	V_{IN}=V_{DD}~V_{EE} (Output SC1-SC40 : floating)	-10	10	µA	V1-V6

AC CHARACTERISTICS (V_{DD}=2.7 ~ 5.5V, V_{DD}-V_{EE}=3 ~ 13V, V_{SS}=0V, Ta=-30 ~ +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2, FLM
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	CL=15pF	-	500		DL1, DL2, DR1, DR2

* Input/Output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".

TIMING CHARACTERISTICS

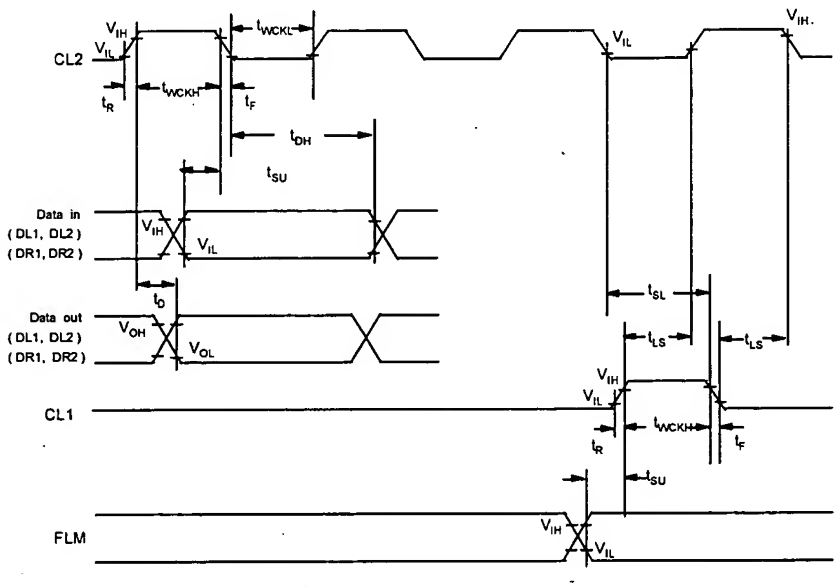


Fig 3. AC characteristics

FUNCTIONAL DESCRIPTION

1) To drive segment type
When the FCS is connected to Vss, KS0065B(SC1-SC40)is operated as segment driver.(refer to Fig 4)

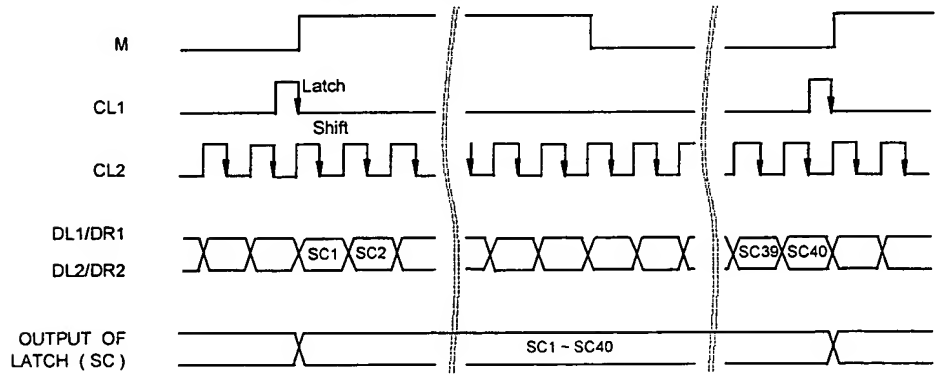


Fig 4. Segment Data Waveforms

2) To drive common type
When the FCS is connected to V_{DD}, only part2(SC21-SC40)of KS0065B is operated as common driver.(refer to Fig 5).

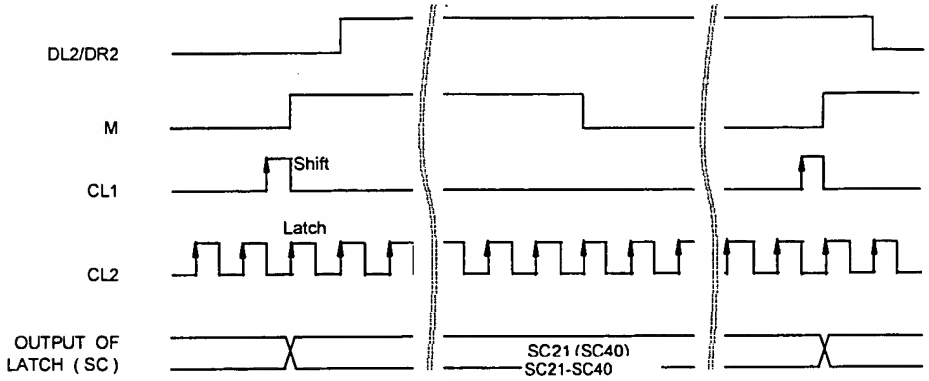


Fig 5. Common Data waveforms

LCD OUTPUT WAVEFORMS

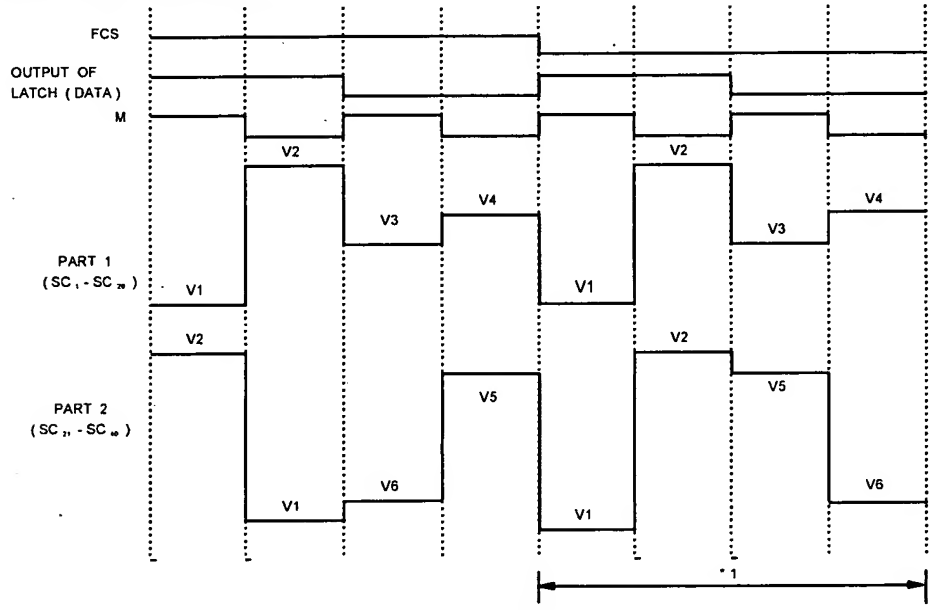


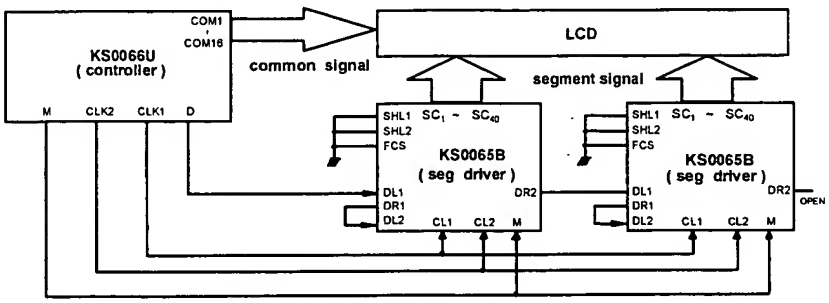
Fig. 6. Output waveform

Fig 6. Output waveforms

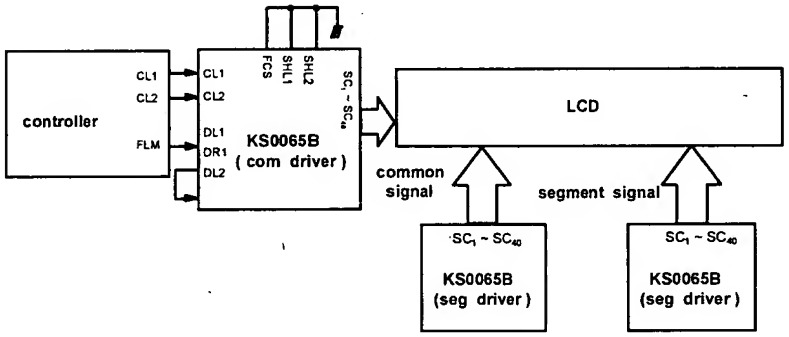
*1: To use for same function of part 1 and part 2, V3 ar ıly for LCD drive are short circuited respectively.

APPLICATION CIRCUIT

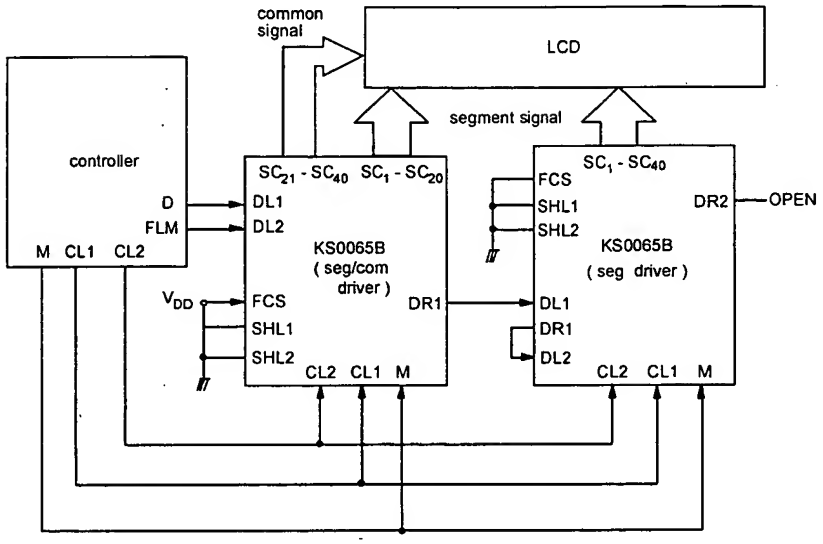
1) Segment driver



2) Common driver



3) Segment/common driver



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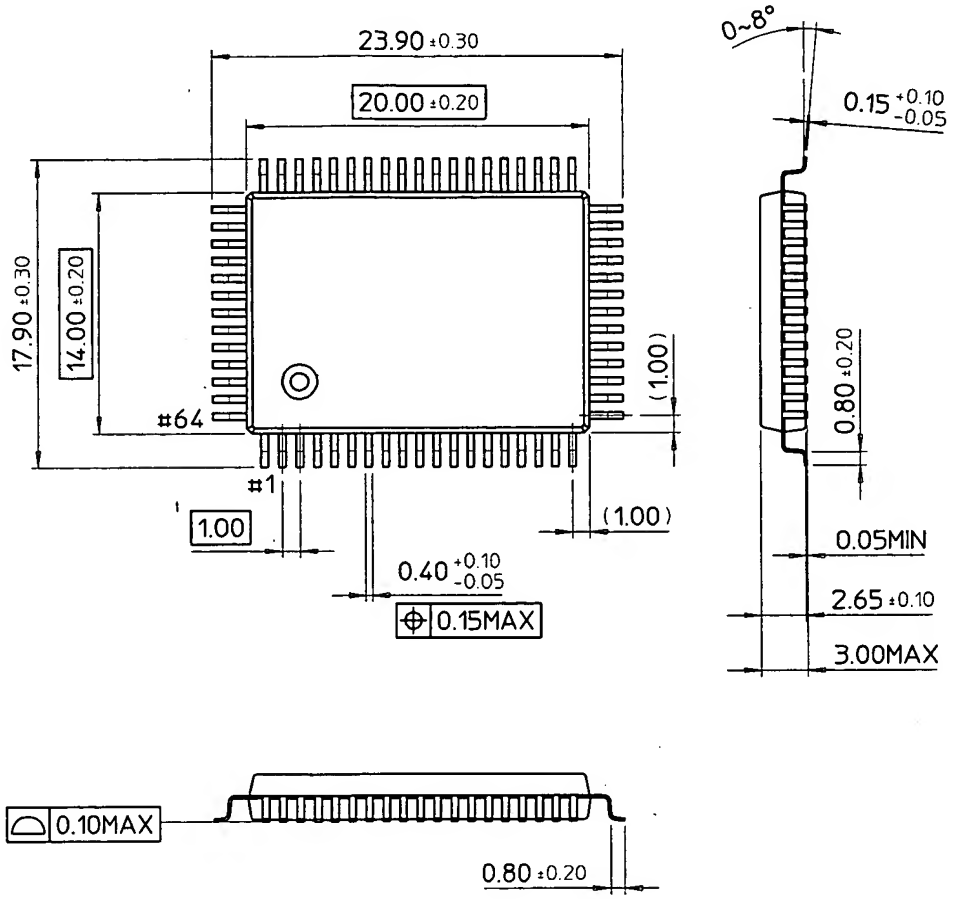
Dimensions in Milimeters



SAMSUNG ELECTRONICS CO.,LTD.